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DEFUZZIFICATION CIRCUIT STANDARD-CELL AND ITS LAYOUT ON CMOS ANALOG INTEGRATED CIRCUIT

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ABSTRACT

This paper presents the design of defuzzification circuit and its layout on CMOS analog integrated circuit. The center-of-gravity method with fuzzy singleton consequences is used to convert fuzzy control actions into crisp control signals. Voltage-follower aggregation circuit is utilized to realize defuzzification circuit. In common applications, it commonly uses three, five, or seven consequences for output fuzzy decision action. The advantageous feature of this circuit is that its consequence values are flexible depending on voltage signals applied to any ports dedicated for consequence external voltage pins. By using single standard-cell technique of voltage follower layout, then it is easy to design and layout the required defuzzification circuit with simple touch. The proposed defuzzification circuit is laid out using 2-micron Scalable CMOS N-well Analog (SCNA) technology process. The core size of the standard-cell is 56×97 μm.

INTRODUCTION

Fuzzy system has three main processes (see Figure 1). Converting state signals or conditional signal into fuzzy information is done by fuzzifier components. Fuzzy inference engine is then processed the fuzzy information to give fuzzy inference decisions. The defuzzifier components convert the fuzzy inference decision into crisp decisions. All the ways of processing the information are based on knowledge base. The knowledge base about system characteristics and its environments must be gained before designing a fuzzy system. That is why, human experts in accordance with system characteristics are required. More information about fuzzy logic and systems can be found in [1).]

The need for speed processing brings hardware realization of fuzzy logic system being best solution in signal processing and industrial applications. There are three approaches in implementing fuzzy hardware: digital [2)] and [3)], analog [4)] and [5)], and mixed-analog-digital mode [6)] and [7)].

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The digital approach gives high flexibility since binary signals used in this mode are easy to program. Several digital storage components such as RAM, ROM, and EPROM are also available for storing knowledge base information of the certain application. Indeed, the digital fuzzy system is easily coupled with existing digital systems. However the digital approach commonly requires large logic gates implying to large silicon area.

The analog approach generally requires much less silicon area than its counterpart digital fuzzy system. There are two basic components, which basically categorize the analog approach. They are bipolar transistors and field-effect transistors. And the approaches to realize fuzzy hardware can be divided into Bipolar, CMOS, and BiCMOS mode. The last mode uses bipolar and CMOS transistor to realize all modular components in analog fuzzy hardware.

The mixed-signal analog-digital combines the advantageous of both digital and analog approaches. Thus this mode uses analog component to realize fuzzy modular component, thus reduce silicon area consumption. And it uses digital component to enhance its flexibility and programmability.

This paper will only cover the design of the defuzzifier component and its layout on CMOS integrated circuit using 2-micron SCNA process technology. This paper is also an advance investigation of our previous paper [8] and [9].

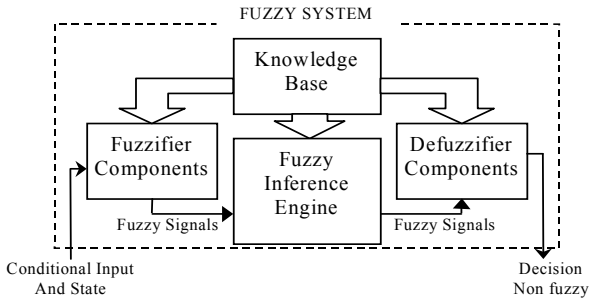


Fig.1. Fuzzy signal processing overview.

In general there are two kinds of output membership function terms: fuzzy membership function or fuzzy singletons. In case of the output terms with fuzzy singleton, Figure 2 shows example of five fuzzy singletons called VS, S, M, L and VL. Designer could easily determine fuzzy singleton position in output's universe of discourse. This approach not only works in high-speed calculation but also it gives simple implementation on circuit, because it cuts the use of transistors massively.

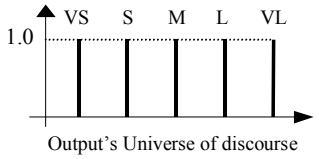


Fig.2. Five fuzzy singleton consequences.

There are several defuzzification techniques that are available. Among other techniques, Center of Gravity method has been widely used in practices and is preferred in this paper. Figure 3 shows a number of *k* graded consequences weighted by inference signals. This is called fuzzy decision or control action. Using center-of-gravity defuzzification method, then the crisp output can be formulated as in equation (1).

$$\text{Crisp\_output} = \frac{\sum_{j=1}^{k} V_{inf-j} \cdot V_{con-j}}{\sum_{j=1}^{k} V_{inf-j}} \qquad (1)$$

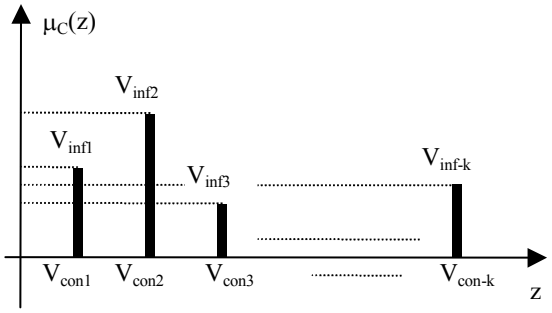


Fig.3. Aggregation diagram resulted from membership functions of inference outputs of Figure 2.

CMOS DEFUZZIFICATION CIRCUIT

Defuzzification circuit (DFC) presented in this paper uses principle of the voltage-follower aggregation circuit. The following sub-section will described the operational principle of that circuit and the realization of the DFC.

1. Principle of voltage-follower aggregation

Defuzzification circuit implementation is based on the principle of a voltage follower-aggregation circuit. Transconductance amplifiers (TCA_1, TCA_2, …, TCA_{k-1}, TCA_k) are used to aggregate the inference voltage V_{con1}, V_{con2}, …, V_{con-k} respectively. By Assuming that the transconductance of an amplifier A_j is G_j, then the current from the *j*th

amplifier A_j to the common point V_{out} is $I_j = G_j(V_j - V_{out})$. See Figure 4 for general diagram of voltage-follower aggregation. Based on Kirchoff's current law, the sum of the currents I_j coming from the k amplifier is zero. It is formulated in the following equation.

$$\sum_{j=1}^{k} G_j\left(V_{con-j} - V_{OUT}\right) = \sum_{j=1}^{k} I_j = 0 \qquad (2)$$

Thus it is simplified as

$$V_{OUT} = \frac{\sum_{j=1}^{k} G_j . V_{con-j}}{\sum_{j=1}^{k} G_j} \qquad (3)$$

The equation above means that V_{out} is the average of V_{con-j} and the contribution of each V_{con-j} to V_{out} is weighted by the transconductance of corresponding amplifier G_j. The transconductance G_j of an amplifier is proportional to the root of the current source when the amplifier operates in its linear region, and the VCC_k converts an input voltage V_{inf-k} into a current I_j with a square law. If we used a voltage to current converter to drive the current source of a transconductance amplifier, then the circuit represents the defuzzified value or crisp output as follows

$$z = V_{OUT} = \frac{\sum_{j=1}^{k} V_{\inf-j} . V_{con-j}}{\sum_{j=1}^{k} V_{\inf-j}} \qquad (3)$$

2. Configuration of the voltage-follower aggregation

Generally configuration of the DFC using voltage-follower aggregation is shown in Figure 4. As mentioned in advance, the one pair of voltage-follower aggregation consists of one transconductance amplifier circuit and one voltage to current circuit. Detail schematic of the DFC or the voltage-follower aggregation circuit is presented in Figure 6 (for three pairs) and Figure 7 (for five pairs).

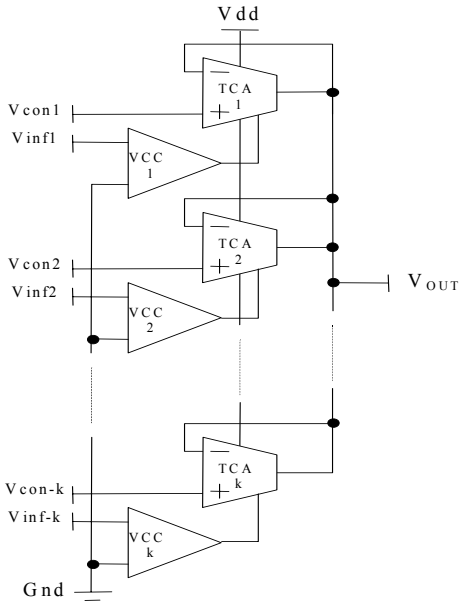


Fig.4. General schematic of defuzzifier circuit with voltage follower aggregation configuration.

The voltage-follower circuit consists of five MOS transistors, two PMOS transistors and three NMOS transistors. That circuit layout of a single voltage-follower can be seen in Figure 5. With this standard cell, the designers could easily design voltage-follower aggregation circuit according to their need. They may design and implement 3, 5, or 7 fuzzy singleton consequences with simple touches.

Table 1 shows the size of gate channel length and width of five transistors on single voltage follower cell using CMOS integrated circuit layout. The transistor is laid out using 2-micron Scalable CMOS N-Well Analog (SCNA) process technology. This database process is used with IC layout tool editor, L-Edit Student Edition Version form Tanner Corp.

Table 1: The transistor sizes.

Transistor		L	W
Name	**Type**		
M1	PMOS	3 μm	14 μm
M2	PMOS	3 μm	14 μm
M3	NMOS	3 μm	22 μm
M4	NMOS	3 μm	22 μm
M5	NMOS	3 μm	10 μm

Note: L = effective gate channel length.
W = gate channel width.

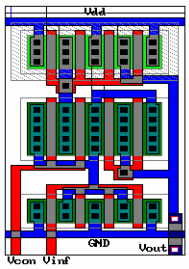
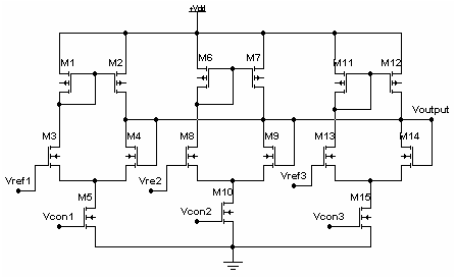
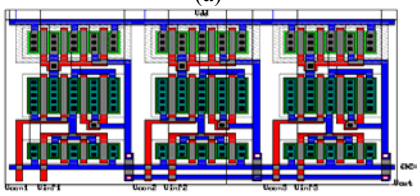


Fig.5. Single voltage-follower standard-cell.

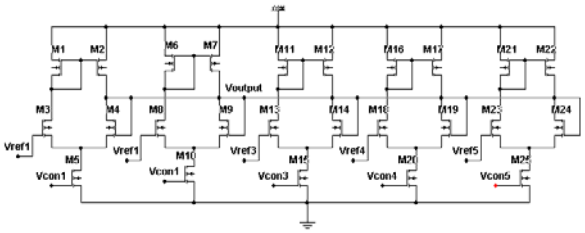


(a)

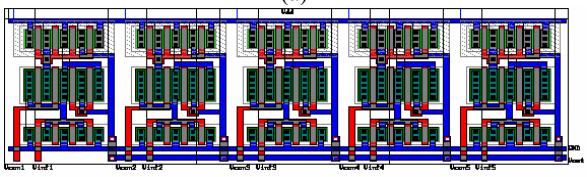


(b)

Fig.6. (a) Three voltage-follower pairs schematic. (b) Its CMOS integrated circuit layout.



(a)



(b)

Fig.7. (a) Five voltage-follower pairs schematic. (b) Its CMOS integrated circuit layout.

SIMULATION RESULTS

The simulation results of the proposed defuzzifier circuit can be observed in Figure 8 – 13. This simulation is undertaken by setting consequence voltages V_{con1}, V_{con2}, V_{con3}, V_{con4}, and V_{con5} with 1, 2, 3, 4, and 5 volt respectively. Figure 8 – 12 shows the simulation results where one of the inference voltages is swept between 0 to 1 volt and the other inference voltages in 0.2 volt. It looks that the output voltage (V_{out}) will tend to move from 4 to the consequence voltage of which its inference voltage is swept. For example, see Figure 12, V_{out} tends to move to V_{con5}=5 V, because V_{inf5} moves to the highest-grade 1 volt. This behavior is accepted in situation that the defuzzification circuit searches for its center of gravity point.

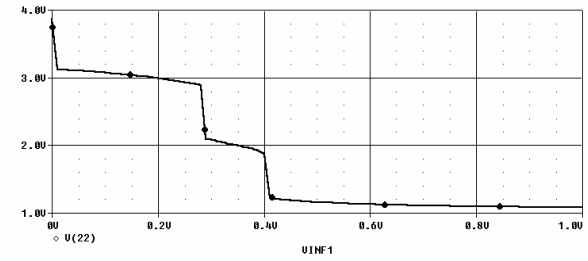


Fig.8. Simulation results with V_{inf1} is swept from 0 to 1 V. V_{inf2}=V_{inf3}=V_{inf4}=V_{inf5} = 0.2 V.

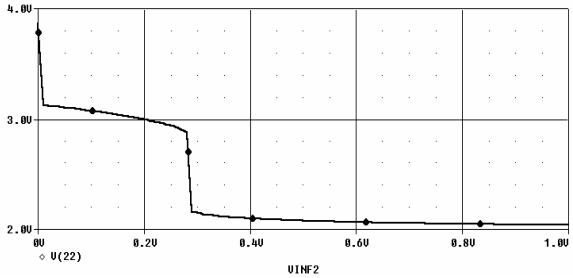


Fig.9. Simulation results with V_{inf2} is swept from 0 to 1 V. V_{inf1}=V_{inf3}=V_{inf4}=V_{inf5} = 0.2 V.

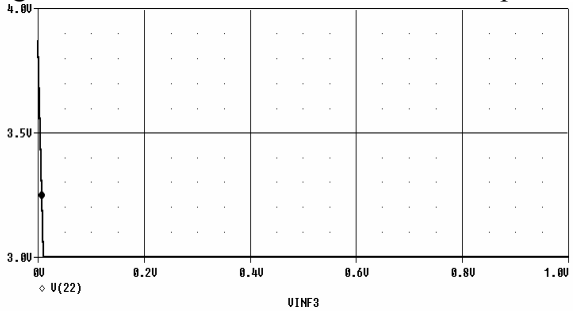


Fig.10. Simulation results with V_{inf3} is swept from 0 to 1 V. V_{inf1}=V_{inf2}=V_{inf4}=V_{inf5} = 0.2 V.

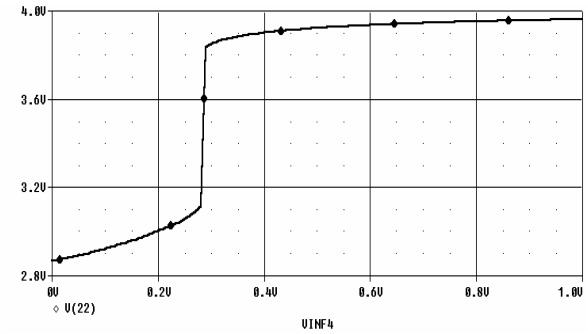


Fig.11. Simulation results with V_{inf4} is swept from 0 to 1 V. V_{inf1}=V_{inf2}=V_{inf3}=V_{inf5} = 0.2 V.

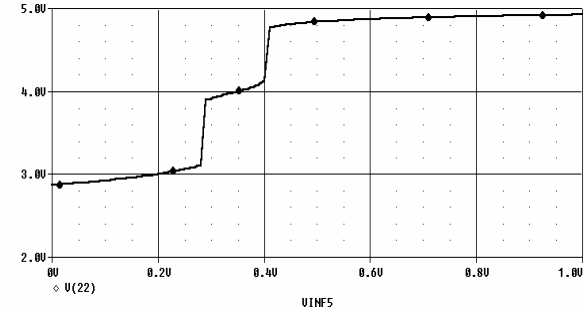


Fig.12. Simulation results with V_{inf5} is swept from 0 to 1 V. V_{inf1}=V_{inf2}=V_{inf3}=V_{inf4} = 0.2 V.

Figure 13 shows the same situation in Figure 12, except that the other consequence voltages are set to 0.5 V. The differences can be observed from its starting point and the slope of their movement. The curve in Figure 12 starts from a few volts below 3 V (2.85 v), while curve in Figure 13 starts from 2.6 V. Another difference between simulation results in Figure 12 and 13 is looked in the slope of the curves. Curve in Figure 13 is more gradual then one shown in Figure 12. This is due to the simulation in Figure 13 is done with all inference voltages except V_{inf5} are set by 0.5 V, it is larger that that of resulted from Figure 12. In defuzzification concepts this result could be accepted. Figure 14 shows the more gradual curve than the that of yielded in Figure 13. It looks that if all inference voltages are set by 1.0 volt, then the output voltage must be 3 volt. Once again this result does make a sense.

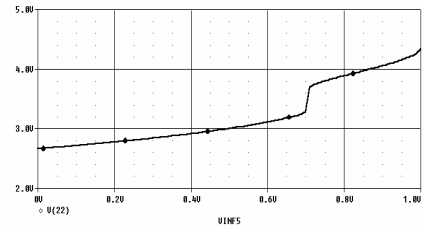


Fig.13. Simulation results with V_{inf5} is swept from 0 to 1 V. V_{inf1}=V_{inf2}=V_{inf3}=V_{inf4} = 0.5 V.

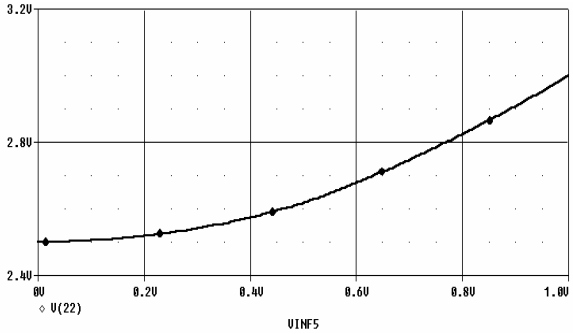


Fig.14. Simulation results with V_{inf5} is swept from 0 to 1 V. V_{inf1}=V_{inf2}=V_{inf3}=V_{inf4} = 1.0 V.

Table 2 shows verification on a few operation points of the defuzzification circuit. The verification is run for consequences values of V_{con1}, V_{con2}, V_{con3}, V_{con4}, and V_{con5} with 1, 2, 3, 4, and 5 volt respectively. The five Inference voltages V_{inf1-5} are set to random values between 0 to 1 volt.

Table 2: Verification of a few operation points.

V_{inf-k} (volt)					Hand-calculate (volt)	Verifi-cation (volt)
k=1	k=2	k=3	k=4	k=5		
1	1	1	1	1	3.0000	3.0000
0.5	1	1	1	0.5	3.0000	3.0000
0.5	1	0.5	1	0.5	3.0000	3.0000
0.5	0.5	1	1	0.5	3.1429	3.3835
0.5	1	1	0.5	0.5	2.8571	2.6165
0	1	1	0.5	0.5	3.1667	2.7532
0.5	1	1	0.5	0	2.5000	2.5000
0.5	0	1	0.5	0	2.7500	3.0000
0.1	0.3	0.5	0.7	1	3.8462	4.5440
0.1	0.3	0.5	0.7	0.9	3.8000	4.3821
1	0.7	0.5	0.3	0.1	2.1538	1.4693
0.9	0.7	0.5	0.3	0.1	2.2000	1.6179
0.9	0.7	0.5	0.3	0	2.0833	1.6006

In Table 2, it looks that some operation points have shown matched value between hand-calculated results and verification results. And some operation points have shown approached value between hand-calculated results and verification results. Although, there are some errors for some operation points, the tendency of the fuzzy circuit output voltage has shown desired computation characteristics.

CONCLUSIONS

The proposed defuzzification circuit has been designed and implemented using 2-micron Scalable CMOS N-Well Analog (SCNA) technology process. Using this technology, the core size of a single standard-cell of the defuzzification circuit is 56×97 μm. And for five cells configuration, the core size is 290×97 μm.

The defuzzification with center-of-gravity method has given acceptable functional I/O behaviors. Although this circuit does not give very accurate calculation, this defuzzifier circuit has given good output tendencies to respond several $V_{con} - V_{inf}$ configurations for verification.

This circuit uses 5-volt voltage supply. The proposed defuzzification has also very low power dissipation. For maximum voltages of V_{inf}, maximum power dissipation of this circuit is about 1.170 mW.

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