ISSN: 1411-4674

Design and Layout of Analog CMOS Standard-Cell Of Fuzzy Membership Function Circuit

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ABSTRACT

Integrated circuit design and layout of CMOS analog fuzzy controller circuit in voltage mode is presented in this manuscript. Membership function circuit is one of the main components in fuzzy circuit. It converts crisp inputs from sensors to give fuzzy information. The proposed MFC has several advantageous features. This MFC can be reconfigured to perform triangular, trapezoidal, S-shape and Z-Shape membership forms. And also the membership forms can be adjusted in terms of its center locations in its universe of discourses, and the slopes of the membership functions. The proposed MFC has been laid out using full-custom techniques to provide standar-cell. And it results in a CMOS MFC standard-cell, which could be then used as a standard component for implementing a number of required MFC in integrated circuit. This layout uses 2-micron SCNA (Scalable CMOS N-well Analog) process technology. The layout results in standard-cell with core size of 120×130 μm.

INTRODUCTION

Fuzzy Logic Controller (FLC) as one of the intelligent control systems has been extensively used in some electronic equipment such as in air conditioner, rice cooker, washing machine, and as automatic transmission controller in automotive. FLC has also intensively applied in process control system both in evaporation control and distillation control. FLC applications in chemical process are for examples in sterilizing process of CPO (crude palm oil) production, pH control in pharmaceutical production, food processing, and so on. There are three main processes of fuzzy system described briefly in the following points:

1. Firstly converting crisp signals from sensors into fuzzy information. The fuzzy information is taken from the grade values related to any membership form of the crisp inputs.
2. Secondly, fuzzy information is processed to give inference signals based on fuzzy rules using fuzzy reasoning technique.

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3. Thirdly, the inference signals are converted back to crisp signals as control action to real actuators.

The understanding of fuzzy sets and fuzzy reasoning are basic knowledge to surf the fuzzy logic theory. Basic explanations of fuzzy sets and fuzzy logic theory can be found in [1]. Fuzzy logic controllers are available implemented on two options: the software and the hardware approaches. Depending on the design technique employed, fuzzy hardware is classified into three groups: digital [2] and [3], analog [4] and [5] or mixed-signals [6] and [7], which combined analog and digital signals for processing the information. The first fuzzy chip was reported in 1986 at AT&T Laboratories (Murray Hill, NJ). Since then many different approaches have been suggested.

The software approach simply consists in programming the desired functions by use of any programming language. A special software tool is usually interfaced to support problem formulation in terms of fuzzy logic. The software approach distinguishes by low cost (not in case of massive products of the electronic appliances), and high flexibility in term of permitting quick and easy alterations. However, the serious disadvantages is the low execution speed of the logical connectivity, which has proven to be far too low for a lot of important applications such embedded control systems.

The demand for high-speed execution of the fuzzy inference made the hardware approach becomes attractive. It has pursued from the beginning of the fuzzy logic boom in mid of the eighties. The fuzzy logic hardware connectivity can be implemented either on analog or digital circuitry. The architecture of such circuit is tailored to the fuzzy inference, which is the essential operation to execute, due to the knowledge-based nature of the fuzzy logic for problem solving.

The digital approach originated from Togai and Watanabe's work, and resulted in some useful chips. Generally a digital fuzzy system is either a fuzzy co-processor, or a general fuzzy processor or a digital ASIC, which contains logic circuits to compute the fuzzy algorithm memories to store fuzzy rules, and generators or look-up tables for membership functions of the input and output variables. Compared to its analog counterpart, digital approach has greater flexibility, easier design automation, and good compatibility with other digital system, a computer for instance. Most of digital systems require ADC and DAC to communicate with sensors and/or actuators. Furthermore, the digital systems are more complex and need larger chip area, e.g., the synthesis of a 4-bit maximum operation in a CMOS unit requires of nearly 100 transistors.

The analog fuzzy logic approach is proposed to get maximum efficiency in term of silicon area, power consumption, and delay time or processing speed. Thus it leads to low cost and high-speed implementation compared to the digital counterpart. A direct interface of the controller to input and output continuous variables is also possible, thus making the circuitry for analog to digital conversion unnecessary.

This paper will only cover the first main process in the fuzzy system as described in advance. The circuit design and layout of the fuzzy membership function circuit is described in Section 3. It is followed by simulation results graphically described in Section 4.

FUZZY SETS AND FUZZIFICATION

In classical set theory, which is based on bivalent logic, a number or object is either a member of a set or not. For example, an object is either large or small. In theoretic terms, it says that the same object cannot simultaneously be a member of a set and its complement. With fuzzy set theory, an object can be a member of multiple sets with a different membership degree of membership in each set. It might be able to allow the same object be considered "large" to some degree and be considered "small" to another degree. The degree of membership of an object in a fuzzy set expresses the degree of compatibility of the object with the linguistic term represented by the fuzzy set. Figure 1 shows an example of two fuzzy sets with different membership functions.

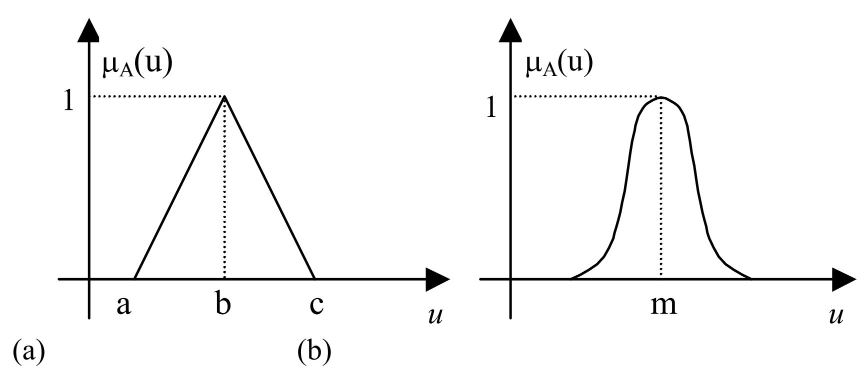


Fig.1. Fuzzy membership functions.

Mathematically Figure 1(a) can be formulated as

$$A = \mu_A(u) = \begin{cases} 0 & ,u < a \\ (u-a)/(b-a) & ,a \le u \le b \\ (c-u)/(c-b) & ,b \le u \le c \\ 0 & ,u > c \end{cases} \qquad (1)$$

While Figure 1(b) can be written as

$$A = \mu_A(u) = \exp\left(-\frac{1}{2}\left\{\frac{u-m}{\sigma}\right\}^2 \right) \qquad (2)$$

A linguistic term is characterized by its term set. The linguistic term speed can be defined by the term set T in the following way: T(Speed)={Slow, Medium, Fast}. T(Speed) denotes the term set of speed, that is, the set of names of linguistic values of speed, with each value being a fuzzy variable, ranging over a universe of discourse.

Three to seven terms are often appropriate to cover a linguistic term. Rarely, one uses less than three terms, since most concepts in human language consider at least the two extremes and the middle in between them. On the other side, one rarely uses more than seven terms because humans interpret technical figures using their short-term memory. The human short-term memory can only compute up to seven symbols at a time. Another observation is that most linguistic variables have an odd number of terms. This is due to the fact that most linguistic terms are defined symmetrically, and one term describes the middle between the extremes. Hence, most fuzzy logic systems use 3, 5, or 7 terms.

Fuzzy linguistic terms can be of several types:

- fuzzy predicates, such as heavy, large, old, small, medium, normal, expensive, near, smart, and the like;
- fuzzy truth values, such as true, false, fairly true, or somewhat true;
- fuzzy probabilities, such as likely, unlikely, very likely, or extremely unlikely;
- fuzzy quantifiers, such as many, few, most, or all.

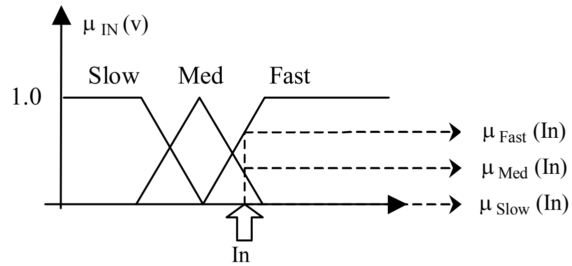


Fig.2. Fuzzification process.

Figure 2 exhibits fuzzification process of a single crisp input over three fuzzy membership terms of "Speed". For every one crisp signal of the input in the universe of discourse, the MFC will give three fuzzified values in accordance with the three membership function forms. As shown in Figure 2, MFC will give μ_{Slow}(In), μ_{Med}(In) and μ_{Fast}(In) for input an input signal.

CMOS ANALOG FUZZY MFC

The proposed MFC circuit consists of 14 MOS transistors. Four of them are PMOS transistors, and the rests are NMOS transistors. The complete circuit schematic is shown in Figure 3. The M1, M2, M3 and M4 perform basic two-pair differential amplifier configuration, which is commonly used to perform membership functions. M11, M12, M13, and M14 perform current mirror configuration, which is used to provide constant current for differential amplifier. M5 and M6 are used as active loads that driving current flow from Vdd (global voltage suplly) through M2 and M3. While M7 and M6 also perform active load for driving output voltage signal. And at last M9 and M10 are utilized as voltage level-shifter and voltage inverter at once. Simulation result of this configuration on three points in the circuit will be exhibited in Section 4.

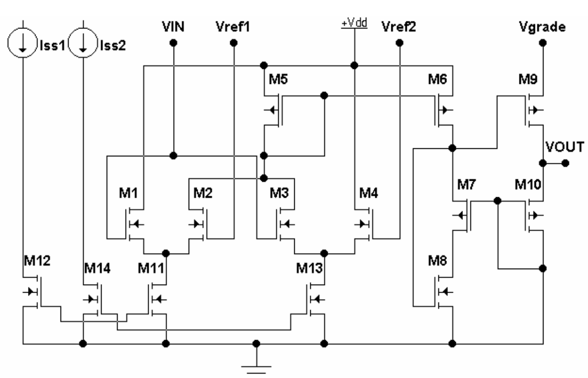
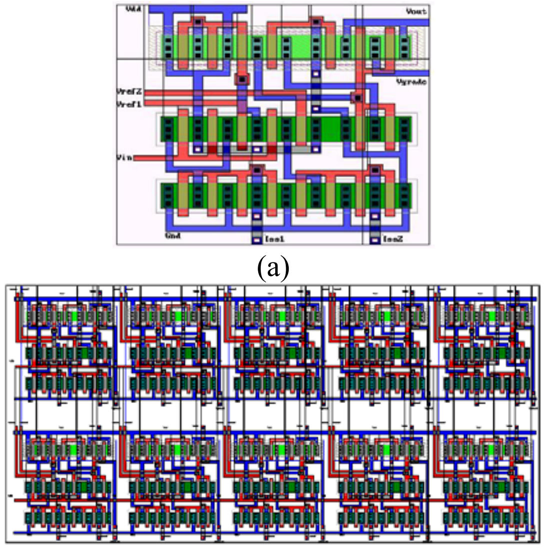


Fig.3. Schematic of CMOS analog fuzzy MFC.



(a)

(b)

Fig.4. Full-custom layout of (a) a single-cell, and (b) ten MFC cells for two inputs.

The MFC has also been laid out using 2-micron SCNA process technology. The circuit layout is done utilizing L-Edit student edition version layout editor from Tanner Corp. A single cell layout result with all transistor have channel length L=4µm and channel width W=14µm, is shown in Figure 4(a). Figure 4(b) shows how to use the single cell to build ten MFC cell with simple touch. All objects in a cell layout are grouped together, then it will perform a standard cell of the MFC. If one would build several membership function forms for a certain input, then it can be done simple by duplicating that standard cell, then place it in the layout editor.

SIMULATION RESULTS

The first simulation results will shows basic characteristic and functional behaviors of the three points in the MFC circuit as mentioned earlier in Section 3. This is shown in Figure 5. Input voltage is swept from 0 to 5 voltage, and voltage at drain point of PMOS5 is shown at upper curve of Figure 5. The middle curve shows the voltage at drain point of PMOS6. It seems that the voltage is inverted and shifting about 5 volt. And the lower curve shows desired output, which performs triangular membership function with 0 V as the lowest membership grade and 500mV as the highest membership grade.

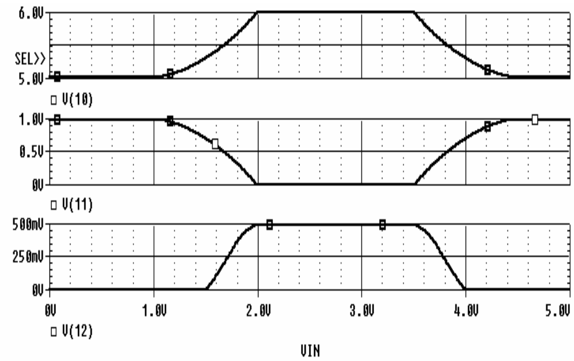
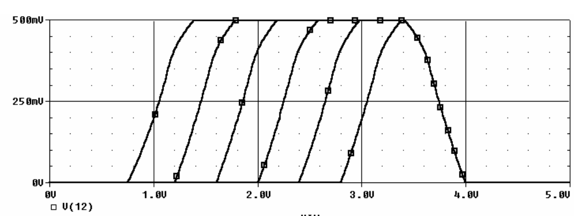


Fig.5. Voltage at the drain of the PMOS M5, M6, and M9 respectively.

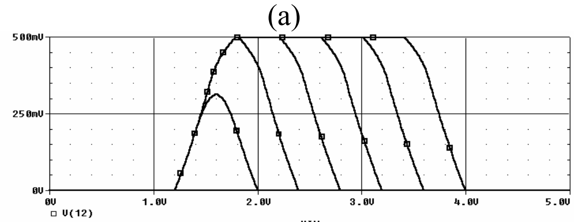
The Triangular and Trapezoidal Forms

The simulation results of the triangular and trapezoidal forms are shown in Figure 6. The triangle forms are obtained by setting Vref1 and Vref2 in different locations in the universe of discourse. Vref1 and Vref2 are denoted in the left-end side and the right-end side of the membership function respectively. Thus in natural, Vref1 should be less than Vref2.

The trapezoidal form is a special case of the triangular one. If one shifts the Vref1 more to the left side then one would obtained trapezoid. This is shown interactively in Figure 6(a). Another case of shifting the Vref2 is shown in Figure 6(b). Note that the gap between Vref1 and Vref2 should be wisely used to guarantee that the highest grade is about 500 mV. This situation can be found in one of the curves exhibited in Figure 6(b).



(a)



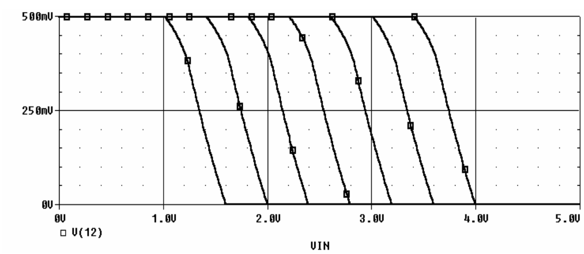
(b)

Fig.6. Trapezoid and triangle form with various (a) Vref1, and (b) Vref2.

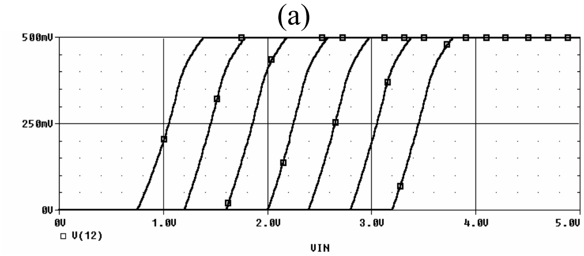
The Z-Shape and S-Shape Forms

The proposed membership function could also perform The Z-Shape and Z-Shape membership function forms as shown in Figure 7 and 8 respectively. The procedure to yield those membership forms is as follow:

- Let Iss1=0 V, then the Z-Shape is obtained. Change the Vref2 to shift the location of the Z-Shape membership function in the universe of discourse. In this condition, Vref1 is no more effectively used.
- Let Iss2=0 V, then the S-Shape is obtained. Change the Vref1 to shift the location of the S-Shape membership function in the universe of discourse. In this condition Vref2 is no more effectively used.



(a)



(b)

Fig.7. (a) Z-form and (b) S-form with various reference voltages.

Grade and Slope Adjustable Forms

The grade and the slope of the membership function can also be adjusted. Changing Vgrade can control the grade of the membership functions. The higher Vgrade the higher the highest grade of the membership function. Figure 8 shows triangular forms with five different grades.

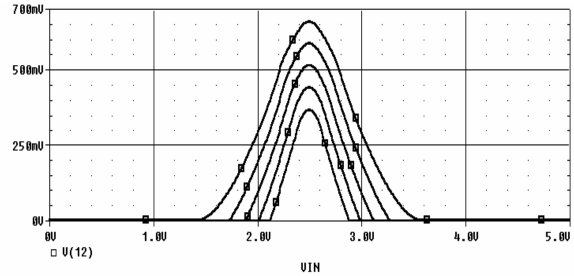
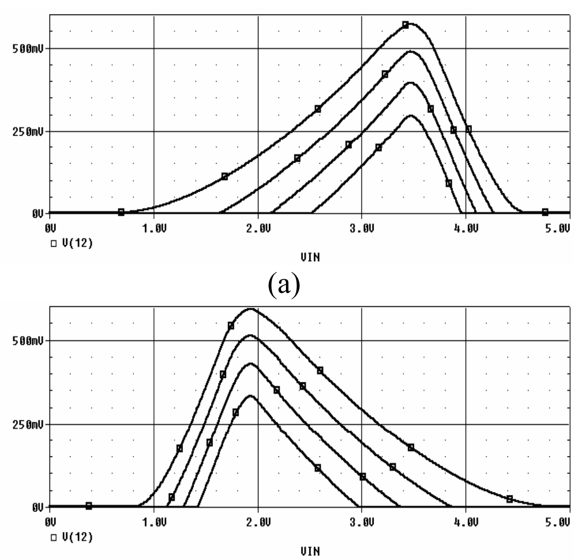


Fig.8. Triangle form with different grade.

The slope of the membership functions can also be controlled. Unfortunately, until this manuscript is proposed, we still control the slope without external currents or voltages. In other words, the slope adjustment is not controlled by current or voltage, but it is adjusted by manipulating the transconductance parameters of the CMOS circuits. These results are shown in Figure 9. Figure 9(a) shows the simulation results of setting the transconductance parameter of M1 and M2 lower than previous simulation results. The lower the transconductance parameters the smaller the slope of the membership function. While the results of Figure 9(b) are obtained by setting transconductance parameters of M3 and M3 lower than previous results. If the one keep lowering the transconductance parameter setting and make the slope small and smaller, then the highest grade of the membership forms start shifting down from 500mV. In this condition, an intervention should be made by adding voltage supply to Vgrade wisely; thus it keeps the highest-grade stay at 500 mV.



(a)

(b)

Fig.9. Triangle form with different grade and (a) left-slope, and (b) right-slope.

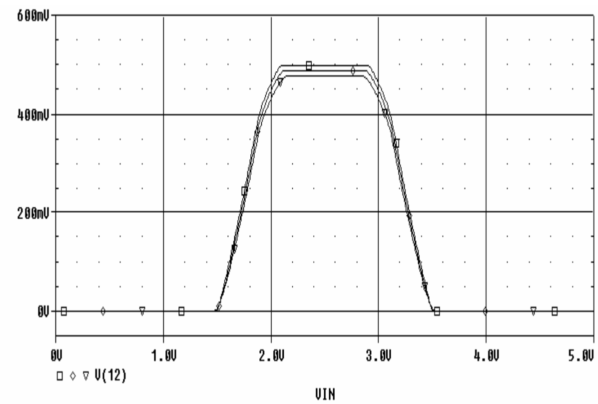


Fig.10. Temperature effect simulation.

Figure 10 exhibits simulation on temperature effects on the functional behaviors of the MFC. The simulation is run with temperature 27^{O}, 47^{O} and 67^{O} C. It looks that the grade of the membership function experiences small reduction in millivolt scale.

CONCLUDING REMARKS

This proposed fuzzy membership function circuit has given flexible handling to perform four types of membership function form: Z-shape, S-shape, triangle and trapezoidal forms. The shape, the grade and position of all membership function types can be reconfigured by changing and setting external current and voltages, which directly perform the modes of membership forms.

The membership function circuit also operates in low power dissipation about 0.1-0.2 mW for 6-volt power supply. It seems that the power dissipation is small enough. This power dissipation value depends on voltage supply and reference voltage of the MFC. This small value gives economic operations of the circuit for long time operation in industrial processes.

The circuit has been laid out using 2-miron SCNA technology process. The standard-cell of the membership function circuit gives the core size of 120×130 μm. This small core size is suitable to design very-large scale fuzzy circuit where fuzzy controller has multi-input multi-output architecture with large number of fuzzy rules.

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